

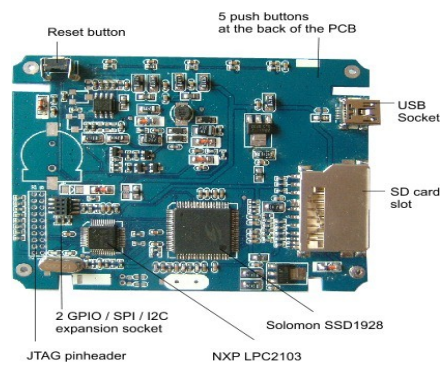
omnima

Advanced automation systems

Embedded controller: 2xUSB, 5xEthernet, 16MB RAM, 1UART, ...



Programmable NXP LPC2103/Solomon SSD1928 LCD Display / Control Panel



Technical overview

Omnima Limited, 176 Kennington Road, Oxford OX1 5PG
Company reg. 06038874, Tel. 08458692601

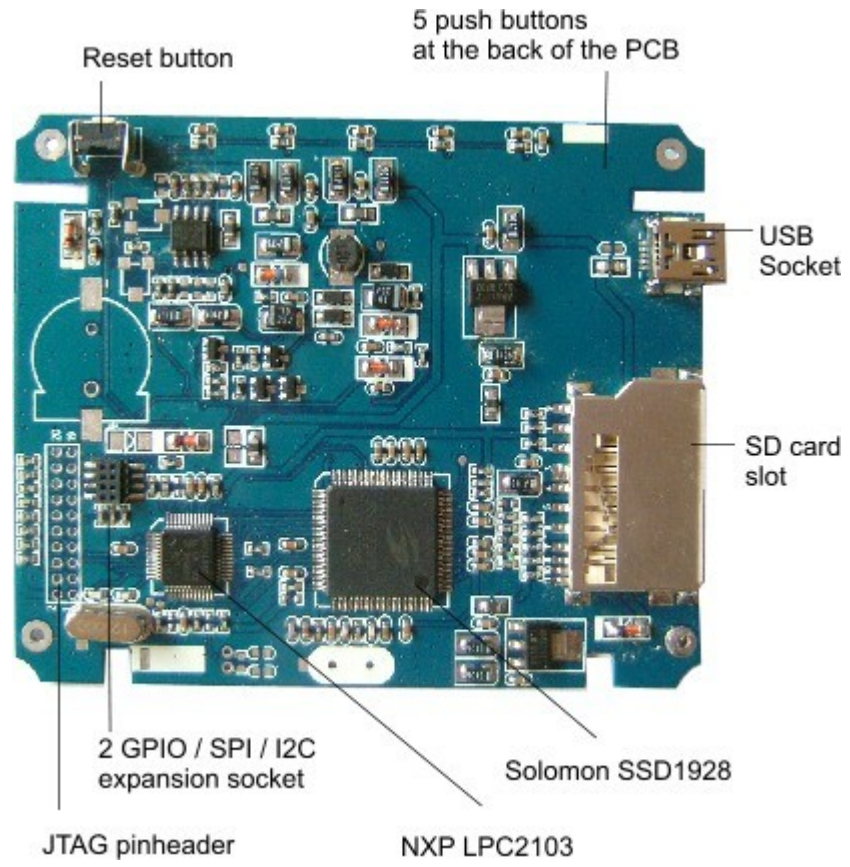
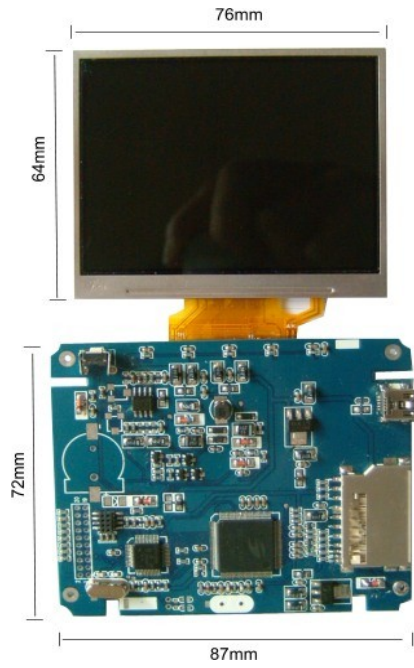
1. Technical details

- NXP LPC2103 based board
- Solomon SSD1928 display controller
- 2 GPIO general purpose I/O ports / SPI or i2C interface
- 1x JTAG programming/debugging port
- SD card reader
- 256KB RAM
- Enclosure size: 100mm x 85mm

2. Main features

- Programmable LCD display
- USB port powered
- Solomon advanced graphics controller with JPEG decompression
- Expansion slot including 2 GPIOs for SPI / I2C connectivity
- Compact case with room for expansion PCBs
- Cost effective

3. Board layout



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CPU

CPU is an LPC2103 ARM7-based MCU. The CPU is clocked at 12MHz, so internally runs at 48MHz.

Graphics controller

The SSD1928 is a fairly advanced display controller. It has a 2D graphics engine featuring panning, scrolling, rotation, line, rectangle and ellipse drawing. There are bit block transfers, and a hardware JPEG engine. The controller supports up to 320x240 in 32-bit colour.

4. JTAG

1: +3.3v supply *	2: +3.3v supply
3: 10k pull-up, ~TRST	4: GND
5: 10k pull-up, TDI	6: GND
7: 10k pull-up, TMS	8: GND
9: 10k pull-down, TCK	10: GND
11: 10k pull-down, RTCK	12: GND
13: 10k pull-up, TDO	14: GND
15: 10k pull-up, ~RST	16: GND
17: 10k pull-down, n/c (DBGRQ)	18: GND
19: 10k pull-down, n/c (DBGACK)	20: GND

* Specifically vref on the JTAG, but same as supply

This is a standard ARM JTAG pin-out and you can use a standard Macgraigor wiggler clone such as the one available from Jabs Place:

http://jabsplace.co.uk/shop/index.php?main_page=product_info&cPath=18&products_id=117.

Backing up/changing the firmware

Under Linux, OpenOCD can be used. Install the latest OpenOcd version. Be sure to follow the config instructions to ensure support for parallel port JTAG.

As root, you need parport modules:

```
modprobe parport
modprobe parport_pc
modprobe ppdev
chmod 777 /dev/parport0
```

Now you can do the rest as a normal user. You can use this config file:

```
#daemon configuration
telnet_port 4444
gdb_port 3333

#interface
interface parport
parport_port /dev/parport0
parport_cable wiggler
jtag_speed 20

#use combined on interfaces or targets that can't set TRST/SRST separately
reset_config trst_and_srst trst_pulls_srst

#jtag scan chain
#Format L IRC IRCM IDCODE (Length, IR Capture, IR Capture Mask, IDCODE)
# Always this for ARM7
jtag_device 4 0x1 0xf 0xe

#target configuration
#daemon_startup reset

#target arm7tdmi <reset mode> <chainpos> <endianness> <variant>
#target arm7tdmi little run_and_init 0 arm7tdmi-s_r4
target arm7tdmi little 0

#run_and_halt_time 0 30
working_area 0 0x40000000 0x2000 nobackup

#flash configuration
flash bank lpc2000 0x0 0x8000 0 0 0 lpc2000_v2 12000 calc_checksum
```

Now run the following command:

```
arm@bomba:~$ openocd -f lpc2103_openocd_wig.cfg &
[1] 2355
Open On-Chip Debugger 1.0 (2008-03-29-00:11) svn:526
$URL: svn://svn.berlios.de/openocd/trunk/src/openocd.c $
Info: jtag.c:1328 jtag_examine_chain(): JTAG device found: 0x4f1f0f0f (Manufacturer:
0x787, Part: 0xf1f0, Version: 0x4)
```

With that lot running in the background you can telnet into the OpenOCD command interpreter and dump the firmware for a backup:

```
arm@bomba:~$ telnet localhost 4444
Trying 127.0.0.1...
Info: server.c:97 add_connection(): accepting 'telnet' connection from 0
Connected to localhost.
Escape character is '^]'.
Open On-Chip Debugger
> dump_image firmware.bin 0 0x8000
dumped 32768 byte in 5.330469s
```

Disassembly

Obtain the GNU ARM tools. The latest Linux binary toolchain at the time of this document going to print was gcc 3.4.3. With the aid of arm-elf-objdump you can get a disassembly:

```

arm-elf-objdump -D --target=binary -marm firmware.bin
firmware.bin:      file format binary

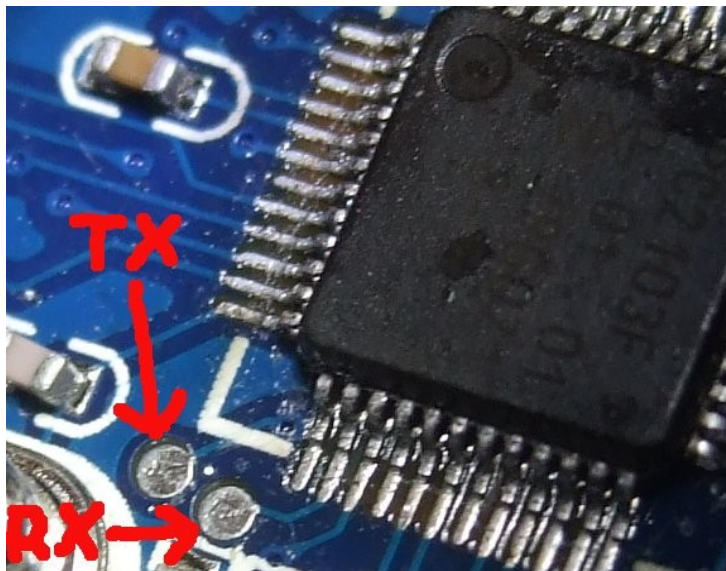
Disassembly of section .data:

00000000 <.data>:
  0:      e59f4034      ldr    r4, [pc, #52]    ; 0x3c
  4:      e3a05002      mov    r5, #2          ; 0x2
  8:      e5845000      str    r5, [r4]
  c:      e3a05003      mov    r5, #3          ; 0x3
 10:     e5845004      str    r5, [r4, #4]
 14:     e59f201c      ldr    r2, [pc, #28]   ; 0x38
 18:     e3a03000      mov    r3, #0          ; 0x0
 1c:     e1020093      swp    r0, r3, [r2]
 20:     e2822028      add    r2, r2, #40     ; 0x28
 24:     e1021093      swp    r1, r3, [r2]
<snip>

```

Console output

For debugging purposes, the pins of one of the LPC2103 UARTs (UART0) are available on two test pads as shown below.



SSD1928 Addressing mode

The interconnections with the LPC2103 are as follows:

```

SSD      ARM
===      ===
M/R#     -> GND
WE1#     -> GND
WE0#     -> P0.21   For 8080, WE#
RD/WR#   -> GND
RD#      -> P0.16
CS#      -> P0.23
D/C#     -> P0.24
DB0:15   -> P0.0:15
RESET#   -> P0.25
PLL_DIS  -> GND

```

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8080 16-bit indirect addressing is therefore configured. There are 16 data/address lines, CS# (chip select), RD# (read strobe), WR# (write strobe) and D/C# (data/command select, pin 47).

6. Power supply

The LCD is powered using a standard mini-USB connector and supply of +5V.

A Schuko power adapter is supplied with the LCD display. A Schuko/UK adapter is also included in the package.

7. Development environment

For information on the development tools and further information please visit:

JTAG cable	http://jabsplace.co.uk/shop/index.php?main_page=product_info&cPath=18&products_id=117
OpenOcd	http://openocd.berlios.de/web/
GNU ARM C tools	http://www.gnuarm.com/
NXP LPC2103 datasheet	http://www.nxp.com/acrobat/datasheets/LPC2101_02_03_2.pdf
SSD1928 datasheet	http://omnima.co.uk/docs/SSD1928_1.0.pdf
SSD192x API Gen	http://omnima.co.uk/docs/SSD1928_1.0.pdf
Sample program	http://linux-adm5120.svn.sourceforge.net/viewvc/linux-adm5120/lpc2103/blink/